Amendment

Please amend the present application as follows.

In the Specification

NE → On page 1, please delete "Luiz M. Franca-Neto".

In the Claims

Please cancel without prejudice claims 13-21 as discussed in a phone conversation regarding a provisional election of claims 1-12.

Please cancel without prejudice claims 1 and 7

Please amend claims 2, 3, 4, 6, 8, 9, 10, 12 to read as provided below. For convenience, all presently active claims are provided below.

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2. (Amended) A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the gate and the first terminal are each connected to the input port, and the second terminal is connected to the output port so that the output voltage is indicative of a local time-average maximum of the input signal voltage; and

wherein in steady state the FET is coupled to operate in a sub-threshold region if the input signal voltage is stationary.

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3. (Amended) A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the gate and the first terminal are each connected to the input port, and the second terminal is connected to the output port; and

wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

4. (Amended) A method to provide an output voltage indicative of a local time-average maximum of an input signal voltage, the method comprising:

operating a field-effect transistor (FET) in its sub-threshold region when in steady state and the input signal voltage is stationary, the FET having a gate, a first terminal, and a second terminal, wherein the gate and the first terminal are each connected to an input port, and the second terminal is connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port.

5. The method as set forth in claim 4, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

6. (Amended) A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the gate and the first terminal are each connected to the input port, wherein the second terminal has a DC offset correction voltage, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width; and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

8. (Amended) A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port so that the output voltage is indicative of a local time-average minimum of the input signal voltage; and

wherein in steady state the FET is coupled to operate in a sub-threshold region if the average voltage is stationary.

9. (Amended) A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port; and

wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

10. (Amended) A method to provide an output voltage indicative of a local time-average minimum of an input signal voltage, the method comprising:

operating a field-effect transistor (FET) in its sub-threshold region when in steady state and the input signal voltage is stationary, the FET having a gate, a first terminal, and a second terminal, wherein the first terminal is connected to an input port, and the gate and the second terminal are each connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port.

11. The method as set forth in claim 10, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

12. (Amended) A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the first terminal is connected to the input port, wherein the gate and the second terminal are connected to each other and have a DC offset correction voltage;